Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Changing the way data is displayed
- Labels for bus cycles
- Viewing disassembled data in various display formats

Acquiring Data

The TCS101 product for the SPI-3 and SPI-4.2 bus installs four different supports: SPI3_TX, SPI3_RX, SPI4, and SPI4_LVTTL.

***NOTE**. The SPI4_Cal and the SPI4_LVTTL_Cal support packages are added for Setup/Hold time adjustments. Use these support packages only when you need to adjust the Setup/Hold time values.*

Use the SPI4_Cal support package for the SPI-4.2 bus with LVDS FIFO Status signals and the SPI4_LVTTL_Cal support package for the SPI-4.2 bus with LVTTL FIFO Status signals.

Once you load the support package, choose a clocking mode, adjust the logic analyzer setup/hold window if required, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help.

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to fit your needs. You can make common and optional display selections in the Disassembly property page.

You can make selections unique to the support package from the TCS101 product to do the following tasks:

- Change how data is displayed across all display formats

- Change the interpretation of disassembled cycles

Optional Display Selections

Tables 2–1 through 2–2 show the disassembly display options for the SPI-3 and SPI-4.2 support packages.

Table 2–1: Logic analyzer disassembly display options for SPI3_TX and SPI3_RX support packages

Description	Option
Show	All (default) Packet
Highlight	All (default)
Disassemble Across Gaps	Yes No (default)

Table 2–2: Logic analyzer disassembly display options for SPI4 and SPI4_LVTTL support packages

Description	Option
Show	All (default) Packet & Control Packet Only
Highlight	All (default)
Disassemble Across Gaps	Yes No (default)

Bus Specific Fields

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Table 2–3 lists the bus specific fields for SPI3_TX and SPI3_RX support packages.

Table 2–3: Bus specific fields for SPI3_TX and SPI3_RX support packages

Field	Definition
Port Address Filter	Choose whether to filter the acquired data sent to or received from a port
Port Address	Enter the port address in hexadecimal
Physical Port Configuration	Select the physical port configuration

Table 2–3: Bus specific fields for SPI3_TX and SPI3_RX support packages (Cont.)

Field	Definition
Cycles	Select cycles to decode data*
Data Bus Width	Select the data bus width in bits
Decode Payload as ASCII	Choose to decode payload information in ASCII

* **Applicable only for the SPI3_RX support package**

Port Address Filter. Select the Port Address Filter as one of the following:

No (default)
Yes

Set this option to Yes if you want to filter the acquired data sent to or received from a selected physical port.

Port Address. Select the Port Address if you want to filter the acquired data sent to or received from the port. The default value is 00.

You can enter a maximum value of FF in hexadecimal for the Port Address.

Physical Port Configuration. Select the Physical Port Configuration as one of the following:

Single - No InBand Addr (default)
Single with InBand Addr
Multiple

For correct disassembly, set the Physical Port Configuration to match with the custom clocking option selected during acquisition.

Cycles. Select the Cycles as one of the following:

All (default)
Active Only

Set this option to All to decode data on every clock cycle, and Active Only to decode data only when the data bus is valid.

For correct disassembly, set the Cycles to match with the custom clocking option selected during acquisition.

***NOTE**. The bus specific field Cycles is used only in the SPI3_RX support package.*

Data Bus Width. Select the Data Bus Width as one of the following:

8 bits (default)
32 bits

Decode Payload as ASCII. Select Decode Payload as ASCII as one of the following options:

No (default)
Yes

Set this option to Yes if you want to see the payload information in ASCII.

Table 2–4 lists the bus specific fields for SPI4 and SPI4_LVTTL support packages.

Table 2–4: Bus specific fields for SPI4 and SPI4_LVTTL support packages

Field	Definition
Port Address Filter	Choose whether to filter the acquired data sent to or received from a port
Port Address	Enter the port address in hexadecimal
Decode Payload as ASCII	Choose to decode payload information in ASCII
Calendar_LEN	Enter the length of the calendar sequence
Calendar_M	Enter the number of times a calendar sequence is repeated between insertions of framing pattern

Port Address Filter. Select the Port Address Filter as one of the following:

No (default)
Yes

Set this option to Yes if you want to filter the acquired data sent to or received from a selected physical port.

Port Address. Select the Port Address if you want to filter the acquired data sent to or received from the port. The default value is 00.

You can enter a maximum value of FF in hexadecimal for the Port Address.

Decode Payload as ASCII. Select Decode Payload as ASCII as one of the following options:

No (default)
Yes

Set this option to Yes if you want to see the payload information in ASCII.

Calendar_LEN. Enter the Calendar_LEN value. You can enter a maximum value of 256 in decimal format. The default value is 1.

Calendar_M. Enter the Calendar_M value. You can enter a maximum value of 256 in decimal format. The default value is 1.

Labels for Bus Cycles

The TCS101 product decodes and displays the bus behavior in the Packet/Cell Details (Mnemonic) column in SPI3_TX, SPI3_RX, SPI4 and SPI4_LVTTL support packages.

Table 2–5 lists the labels displayed in the Packet/Cell Details column in the listing window for the SPI3_TX and SPI3_RX support packages.

Table 2–5: Labels in Packet/Cell Details column for SPI3_TX and SPI3_RX support packages

Label	Description
INVALID DATA	Invalid data on the SPI-3 data bus
PORT ADDRESS : (*Port Address in hex*)	Physical port address
UNRECOGNIZED DATA	Control group value of an acquired sample does not match the control symbol table
SHORT LENGTH PACKET	Packet data at which EOP and SOP signals asserted at same clock edge
ERRONEOUS PACKET	Packet data at which the TERR or RERR signals are asserted
START OF PACKET	Packet start
END OF PACKET	Packet end
PAYLOAD : (*Index in decimal*) : (*Hex value of the payload*)	Packet data

Table 2–6 lists the labels displayed in the Packet/Cell Details column in the listing window for the SPI4 and SPI4_LVTTL support packages.

Table 2–6: Labels in Packet/Cell Details column for SPI4 and SPI4_LVTTL support packages

Label	Description
START OF PACKET (ADDR: *port address in hex*)	Packet start
END OF PACKET (ADDR: *port address in hex*)	Packet end
PACKET CONTINUES (ADDR: *port address in hex*)	Packet continuation
VALID CONTROL WORD	Valid control word
IDLE CONTROL WORD	Idle control word
TRAINING	Training word
Type : (*Control word type*)	Control word "Type"
Port Address : (*Port address in hex*)	Physical port address
DIP-4 : (*DIP-Value*)	Diagonal Interleaved Parity Calculation (4-bit)
PAYLOAD (*Index in decimal*) : (*Hex value of the Payload*)	Payload details

Table 2–7 lists the labels displayed in the FIFO Status column in the listing window for the SPI4 and SPI4_LVTTL support packages.

Table 2–7: Labels in FIFO Status column for SPI4 and SPI4_LVTTL support packages

Label	Description
STARVING	Transfer up to Max Burst 1
HUNGRY	Transfer up to Max Burst 2
SATISFIED	FIFO is almost full
SYNC	Calendar follows
DISABLED	Disabled
TRAINING	–
DISABLED/TRAINING	Unidentified FIFO Status
DIP-2	Diagonal Interleaved Parity Calculation (2-bit)
CAL[*Calendar_LEN index in decimal*]:	Calendar length prefixed to STARVING, HUNGRY or SATISFIED

Viewing Disassembled Data

You can view disassembled data for the SPI3_TX and SPI3_RX support packages in two display formats:

All
Packet

You can view disassembled data for the SPI4 and SPI4_LVTTL support packages in three display formats:

All
Packet & Control
Packet Only

Always select the All display format for viewing correctly disassembled FIFO Status data.

The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–5.*

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

All Display Format in SPI3_TX and SPI3_RX

In this option, all valid and invalid data is acquired at the rising edge of the data clock and displayed.

Packet Display Format in SPI3_TX and SPI3_RX

In this option, all valid packet data is acquired at the rising edge of the data clock and displayed.

All Display Format in SPI4 and SPI4_LVTTL

In this option, all the decoded information is displayed. Figure 2–1 shows an example of the All display format for the SPI4 support package.

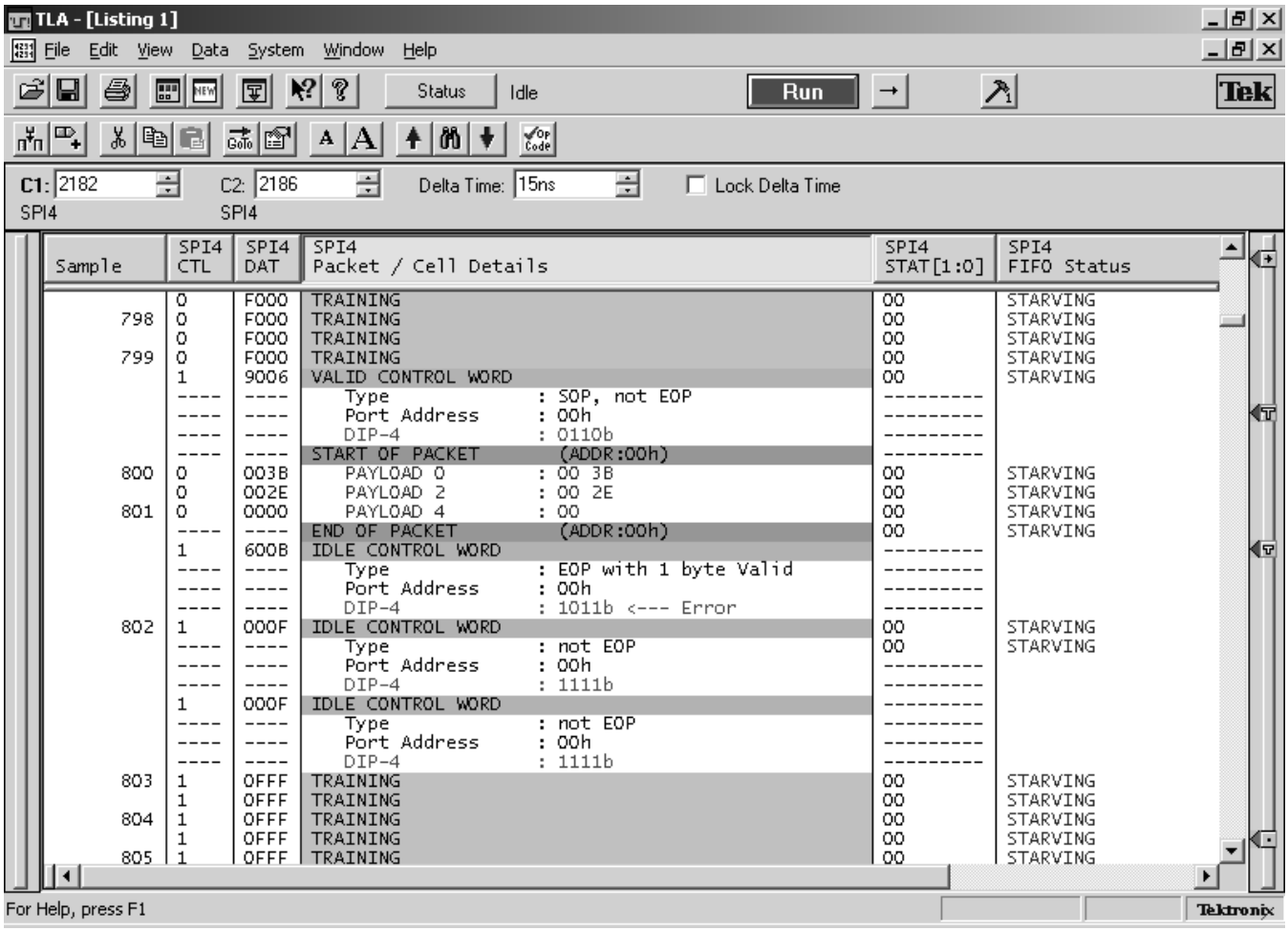

Figure 2–1: Example of All display format for the SPI4 support package

Packet & Control Display Format in SPI4 and SPI4_LVTTL

In this option, the information related to packets and control words, are decoded and displayed. Training related information is not shown.

Figure 2–2 shows an example of the Packet & Control display format for the SPI4 support package.

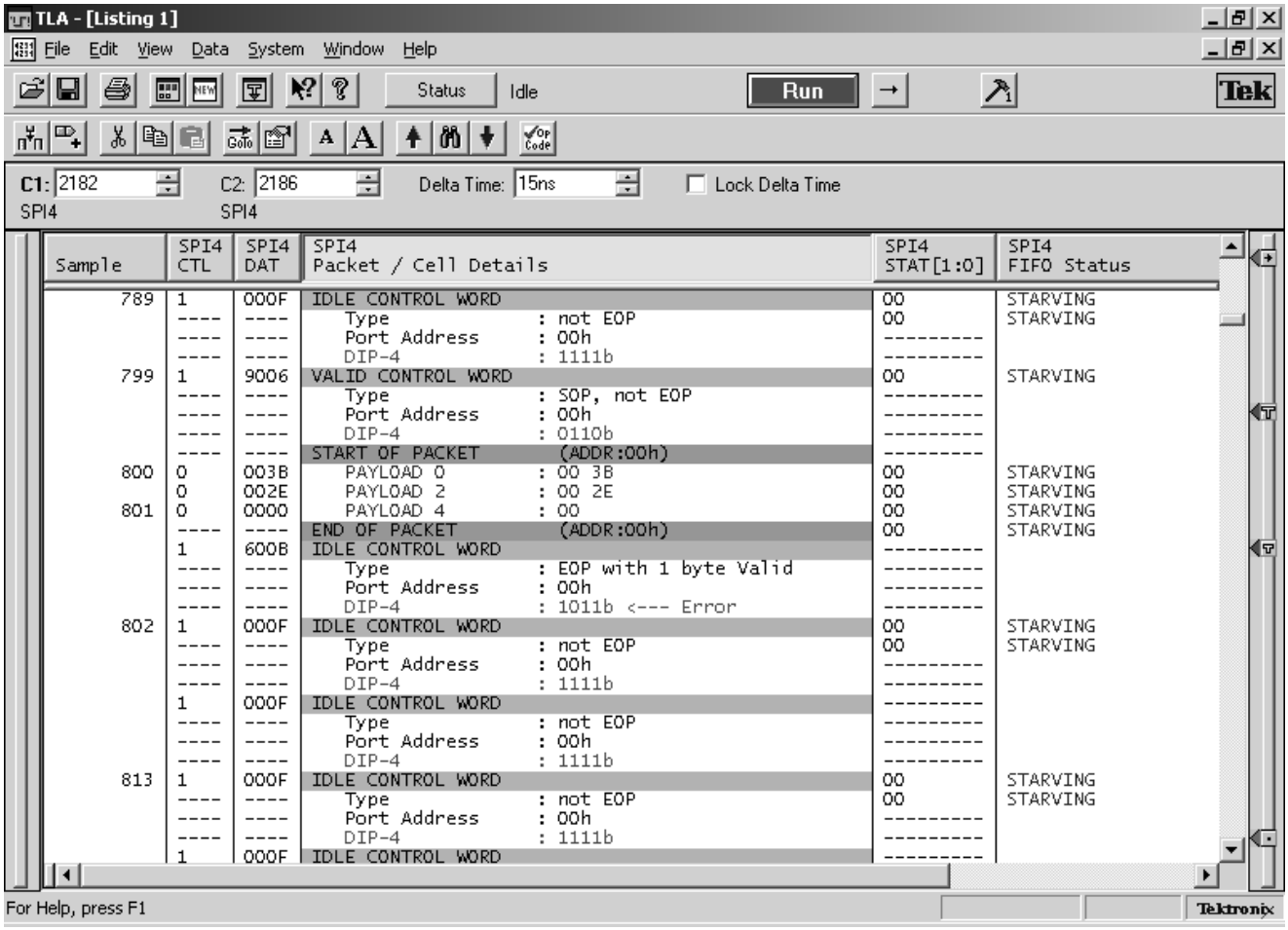

Figure 2–2: Example of Packet & Control display format for the SPI4 support package

Packet Only Display Format in SPI4 and SPI4_LVTTL

In this option, the information related to only packets are decoded and displayed. Other information related to control words is not displayed.

Figure 2–3 shows an example of the Packets Only display format for the SPI4 support package.

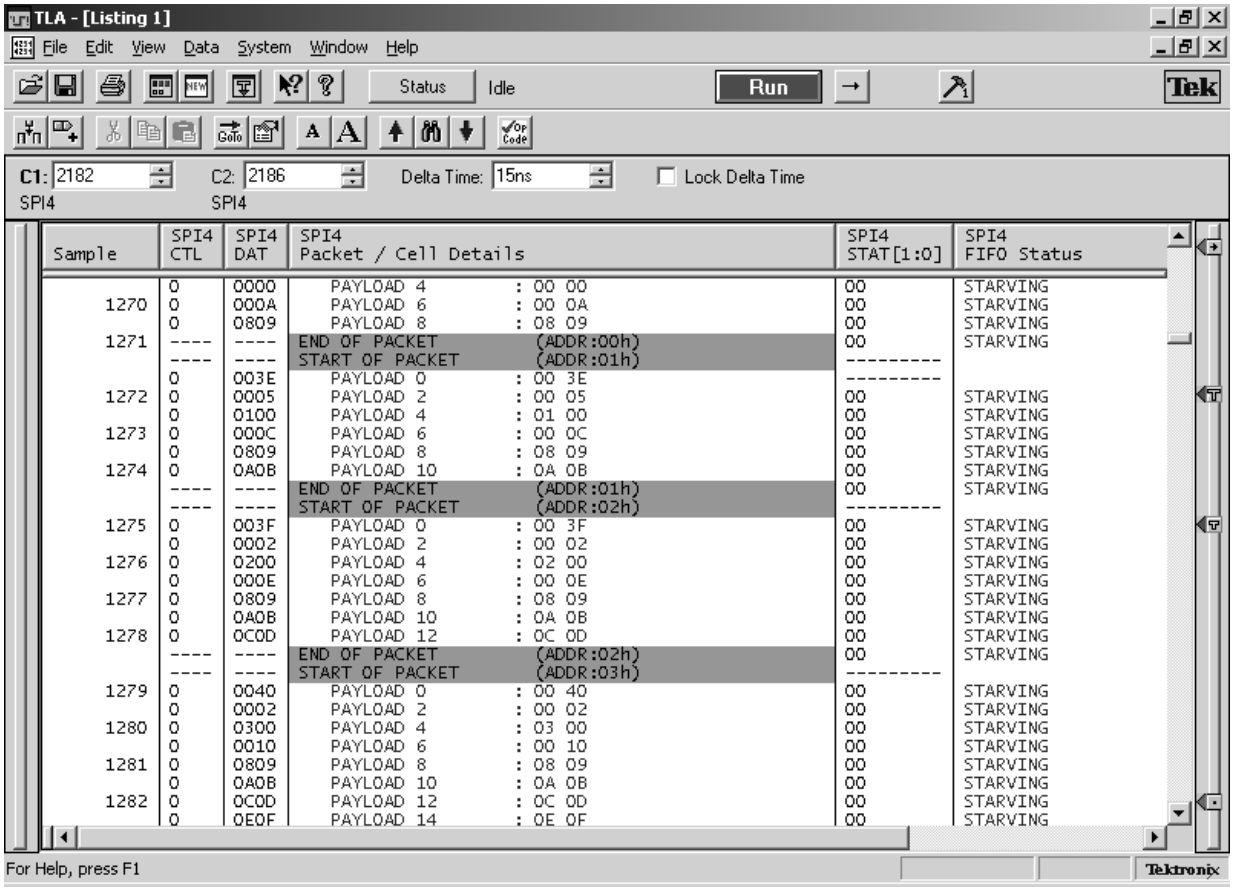

Figure 2–3: Example of Packet Only display format for the SPI4 support package

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your CD-ROM to view an example of how the SPI-4.2 bus cycles look when they are disassembled. Viewing this system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your target system.

Information on basic operations describes how to view the file.